METHOD AND APPARATUS FOR DETERMINING A PROCESSING SPEED OF AN INTEGRATED CIRCUIT

ABSTRACT

A method and apparatus for determining a processing speed of an integrated circuit includes a first flip flop having an input port receiving an input signal, an output port providing a flip flop output signal and a timing port receiving an incoming clock signal. The method and apparatus further includes a delay circuit operably coupled to the output port of the first flip flop, such that the delay circuit receives the flip flop output signal, generating a delayed timing signal. Further included is at least one clock speed adjusting circuit operably coupled to the delay circuit and a multiplexer coupled to the at least one clock speed adjusting circuit and the delay circuit, wherein the multiplexer receives a select delay signal in a selective delay input port. Based on the select delay signal, a multiplexer output signal is chosen and provided to an input port of a second flip flop.